A Low Noise 9.95/10.66 GHz PLO For Optical Applications

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Abstract --- **A 9.95/10.66 GHz monolithic low noise phase-locked oscillator (PLO) implemented in an InGaP HBT technology is presented. It consists of a voltage-controlled oscillator (VCO), a digital phase frequency detector (PFD) and digital frequency dividers. The reference frequency input can be in two ranges, 155 to 167 MHz (divided by 32 selected) or 620 to 668 MHz (divided by 8 selected). Two auxiliary outputs at 4.975/5.33 and 2.4875/2.665 GHz are provided. A PLO phase Noise of –122 dBc/Hz is achieved at 10 kHz offset. The phase jitter is 20.3 fs rms in 10kHz to 10MHz. The MMIC dissipates 1.5 W with two power supplies, +3V for the VCO and +5V for the rest of the circuitry.**

I. INTRODUCTION

Low phase noise signal sources are a key element in many microwave and millimeter wave applications. Modern communication links employing complex modulation techniques require ever better performance from their LO sources in order to achieve low bit error rate. High performance optical communication systems rely heavily on precise clock timing to combine multiple lower frequency data paths into one very wide bandwidth channel suitable for optical transmission. On the receive end, the recovery of this precise clock for use in de-muxing these multiple data channels is also critical to the preservation of the data integrity. High quality clock generation for the above purposes has historically been found to be beyond the range of monolithic implementation. This paper describes the performance of a phase-locked oscillator realized in a GaAs InGaP HBT process with performance close to that achieve with a dielectric resonator oscillator (DRO). The MMIC has the following integrated components: the VCO with integrated resonator and varactors, the programmable divide down chain and the low noise phase-frequency detector. The advantage of this type of solution over previous non-MMIC solutions is that it is low cost, compact and readily integrated into a PCB. The phase noise performance of the VCO and PLO are believed to be the lowest reported to date for an integrated MMIC solution with comparable frequency and tuning range [1]-[5].

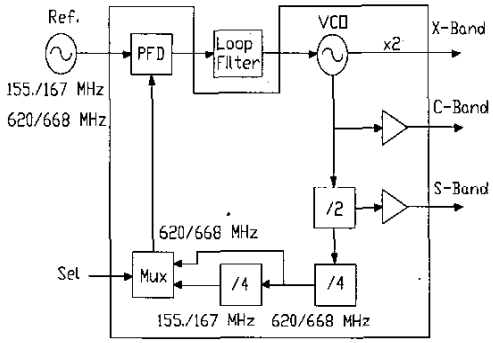

Figure 1. Block diagram of PLO

II. ARCHITECTURE

This 9.95/10.66 GHz monolithic low noise phase-locked oscillator (PLO) is implemented in an InGaP HBT technology. It consists of a voltage-controlled oscillator (VCO), a digital phase frequency detector (PFD) and digital frequency dividers. A block diagram of the PLO MMIC is shown in figure 1. An external Op-amp is used for the loop filter. A high performance push-push VCO has outputs at both X and C-bands. The C-band signal is also divided by two, buffered, and provided as an output at S-band. Then, the S-band signal is divided by 4 or 16 to produce either 620 to 668 MHz or 155 to 167 MHz. The signal from this divider is fed to one input to the phase-frequency detector, the other input of the PFD is provided by the external reference. The output of the PFD feeds the input of an external loop amplifier. The loop bandwidth of the external loop filter can be adjusted to optimize the overall phase noise and jitter performance.

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A. Voltage-Controlled Oscillator (VCO)

The VCO is a fully monolithic X-band design with an output amplifier at the half frequency (C-band). A Colpitts, push-push oscillator topology is selected for the VCO with a distributed tank circuit and on-chip c-b junction varactors. The VCO draws approximately 160 mA from a 3V supply at room temperature. A +5 dBm output power is achieved at 10 GHz. The free running VCO achieves –110 dBc/Hz at a 100 kHz-offset frequency at X-band. The frequency, sensitivity, X-band phase noise plots at room temperature are shown in Figure 2, Figure 3, Figure 4 respectively.

The VCO's phase noise performance is excellent due to the use of high-Q, low impedance distributed transmission lines and high power excitation.

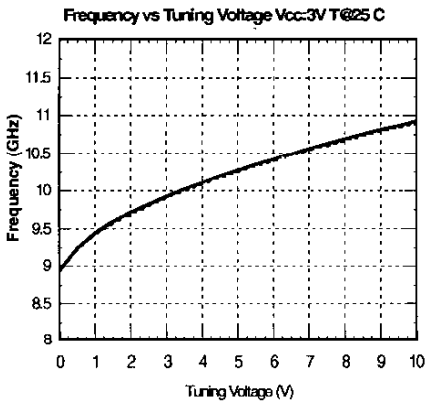

Figure 2. Frequency vs. Tuning Voltage

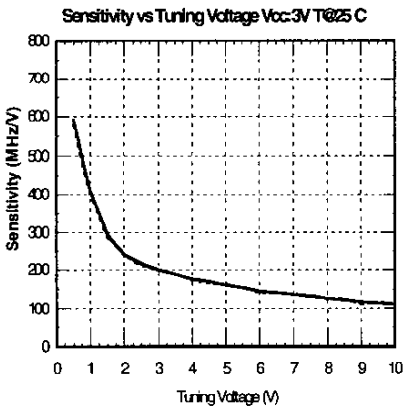

Figure 3. Sensitivity vs. Tuning Voltage

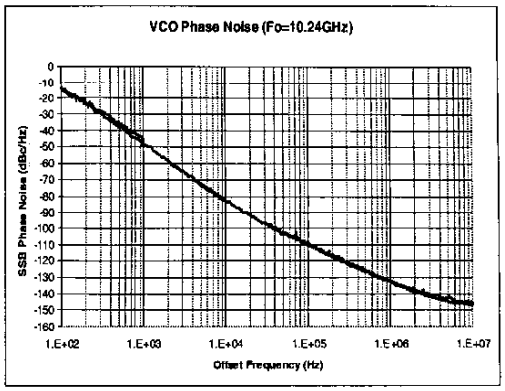

Figure 4. VCO Phase Noise

B. Phase Frequency Detector (PFD)

Initially, the digital phase frequency detector operates as a frequency discriminator for large differences between the reference and VCO input frequencies, and then performs as a coherent phase detector once the frequencies are within the pull-in range of the PLL. The digital phase-frequency detector includes input buffer circuitry, which provides fast rise times to the PFD core logic, and programmable output current, which allows for adjustable gain and increased flexibility when interfacing to an op-amp based active filter. The maximum operating frequency is 1.3 GHz, and the output swing to the active filter is 2 Volts. The core logic operates at a supply voltage of +5V and the current draw is 95 mA.

One key feature of the PFD is immunity to reference input power level. The phase noise floor remains constant while the reference input power level changes from -10 to + 10 dBm. Figure 5 shows the measured output voltage of the PFD versus phase shift between the reference and VCO input ports measured at a 50 MHz input frequency. The data shows excellent linearity and absence of any "dead-zone". The noise floor for a 640 MHz input frequency at 10 kHz offset is approximately -147 dBc/Hz. Table 1 shows a comparison of key performance parameters of the integrated digital PFD versus a commercially available part from Motorola. Since the phase noise floor performance of PFD generally degrades with input frequency at 10 dB per decade, we have normalized the data to 1 Hz, in order to show the relative performance between manufacturers where noise floor data has been characterized at different reference frequencies.

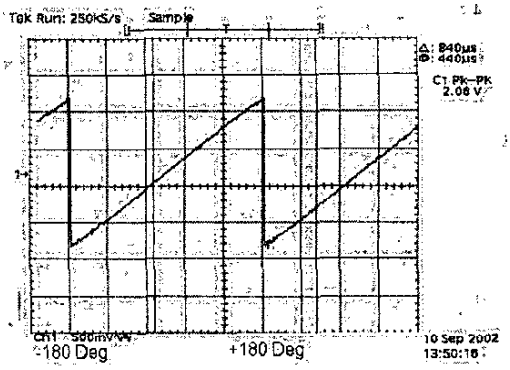

Figure 5. Measured output voltage of the digital PFD at 50 MHz input frequency.

Parameter	Motorola MC12140	Hittite Integrated PFD
Max. Frequency	>800 MHz	>1.3 GHz
Phase Noise Floor Normalized to 1Hz@10K offset	-228 dBc/Hz	-235 dBc/Hz
Current @ 5V	52mA	95 mA
Gain	0.16 V/rad	0.32 V/rad

Table 1. Comparison of key performance parameters of a commercially available PFD versus the integrated PFD used in this PLO

C. Frequency Divider

The digital frequency divider consists of three asynchronous stages (divide-by-2, 4, 4) to achieve the desired divide ratios (Fig. 1.). Each of these stages consists of a master-slave D-type flip-flop with feedback from inverted output to the data input. The flip-flops are realized in emitter-coupled logic (ECL) using series gating between clock and data inputs (Fig. 6.)

The digital frequency divider uses differential signals and +5V power supply. The input frequency can operate up to 8 GHz. The input signal dynamic range is more than 20dB over a wide frequency range. The SSB phase noise is -150dBc/Hz at 100kHz offset frequency.

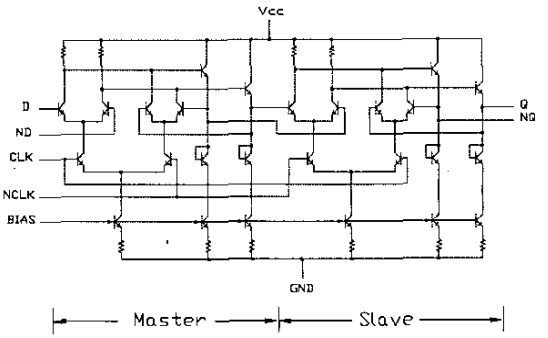

Figure 6. Master-slave flip-flop

III. EXPERIMENTAL RESULTS

The PLO is fabricated in a standard 2um InGaP HBT digital process. The die size for PLO is 2.65mm x 2.35mm. The measurements of the PLO were performed with the chip on the test board directly (Figure 7). The schematic of the test board is shown in Figure 8. An external op-amp with surrounding resistors and capacitors is used for the active loop filter. The values of these components are determined by the system requirements and the relative performances of the VCO, PFD, reference signal and divider ratios. Several examples of input reference frequencies and loop bandwidths are given to illustrate the flexibility of the PLO MMIC. To illustrate the phase noise performance, a low noise 640MHz signal is applied to the reference port of the PLO, the divider ratio is set to 8 and a wide loop bandwidth (500 kHz) is implemented. In this case, the noise floor of the PFD dominates the noise performance inside the loop bandwidth. The resulting phase noise at 10.24GHz is –122 dBc/Hz at 10kHz offset. The phase jitter is 20.3 fs rms in 10kHz to 10MHz. In another case, a low noise 160MHz signal (640MHz divided by 4) is applied to the reference port of the PLO, the divider ratio is set to 32 and the loop bandwidth is the same as before. The resulting phase noise at 10.24GHz is –116dBc/Hz at 10 kHz offset. In cases where the narrow loop bandwidth is implemented, the VCO noise outside the loop bandwidth dominates the noise spectrum. The measured results of the PLO phase noise are shown in Figure 9. For these measurements, we mixed the outputs from two identical units to cancel the reference noise contribution. The main features of the PLO are shown in the table 2.

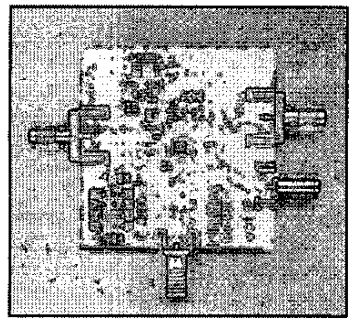

Figure 7. MMIC PLO Chip on Board

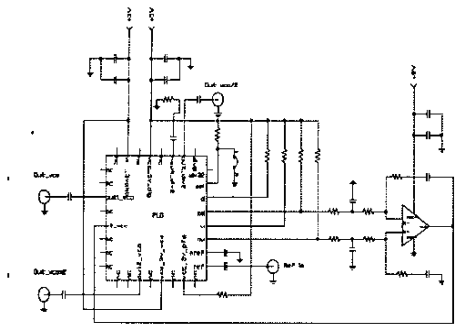

Figure 8. Schematic of PLO test board

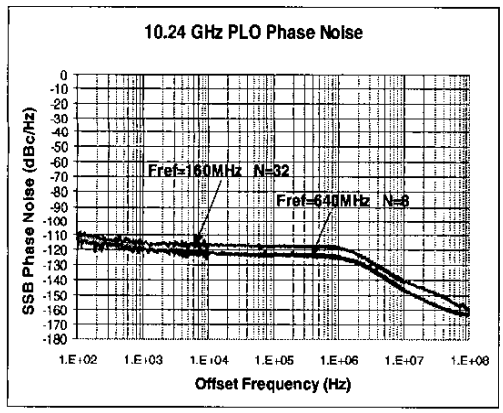

Figure 9. PLO Phase Noise

IV. CONCLUSION

A 9.95/10.66 GHz monolithic low noise phase-locked oscillator (PLO) implemented in an InGaP HBT technology has been developed. An excellent phase noise of -122 dBc/Hz is achieved at 10 kHz offset. The phase jitter is 20.3 fs rms in 10kHz to 10MHz. The PLO MMIC dissipates 1.5 W. The divider ratios are selectable for high or low reference inputs. The combination of high integration, low phase noise, reference frequency flexibility, and low cost makes this PLO very attractive for optical applications.

Output Frequency and Power		
Freq. Band	Fout	Pout
X-Band	10.24 GHz	+5 dBm
C-Band	5.12 GHz	+6 dBm
S-Band	2.56 GHz	0 dBm
Power Supply		
	Vcc	Icc
VCO	+3 V	163 mA
Digital Circuits	+5 V	202 mA
Phase Jitter and Phase Noise at 10.24GHz		
Reference Freq.	Phase Jitter (10kHz~10MHz)	Phase Noise @10kHz
640MHz	20.3 fs rms	-122 dBc/Hz
160MHz	39.3 fs rms	-116 dBc/Hz

Table 2. PLO MMIC Features

ACKNOWLEDGMENT

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